NOV 1 0 2003 PTO/SB/21 (08-03) Approved for use through 08/30/2003. OMB 0651-0031 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE Under the Paperwork Reduction Act of 1995. red to respond to a collection of information unless it displa-**Application Number** 09/654,643 **TRANSMITTAL** Filing Date September 5, 2000 FORM First Named Inventor Pak Shing Chau Art Unit Technology Center 2600 2631 (to be used for all correspondence after initial filing) Examiner Name Bayard, Emmanuel Attorney Docket Number RA-194 Total Number of Pages in This Submission **ENCLOSURES** (Check all that apply) After Allowance communication Fee Transmittal Form Drawing(s) to Technology Center (TC) Appeal Communication to Board Licensing-related Papers of Appeals and Interferences Fee Attached Appeal Communication to TC Petition (AppealN otice, Brief, Reply Brief) Amendment/Reply Petition to Convert to a Proprietary Information After Final Provisional Application Power of Attorney, Revocation Status Letter Affidavits/declaration(s) Change of Correspondence Address Other Enclosure(s) (please Terminal Disclaimer Extension of Time Request Identify below): Return Receipt Postcard Request for Refund Express Abandonment Request CD. Number of CD(s) Information Disclosure Statement Remarks Certified Copy of Priority Document(s) Response to Missing Parts/ Incomplete Application Response to Missing Parts under 37 CFR 1.52 or 1.53 SIGNATURE OF APPLICANT, A TTORNEY, OR AGENT Firm Silicon Edge Law Group LLP - Arthur J. Behiel, Patent Attorney Individual name Signature Date October 28, 2003 CERTIFICATE OF TRANSMISSION/MAILING

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This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C.1 22 and 37 CFR 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. A ny comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sentto the Chief Information Officer, U.S.P atent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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NOV 1 0 2003 35

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Complete (if applicable))

Date

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# FEE TRANSMITTALE for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT

(\$) 180.00

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Co	emplete if Known
Application Number	09/654,643
Filing Date	09/05/00
First Named Inventor	Pak Shing Chau
Examiner Name	Bayard, Emmanuel
Art Unit	2631 RECEIVE
Attorney Docket No.	RA- 194

METHOD OF PAYMENT (check all that apply)				FEI	ECALCULATION (continued) 0V 1 4 2	003.
Check Credit card Money Other None			ONAL Small		Looppology Con	ter 260
Deposit Account:	Fee Code		Fee Code	Fee (\$)	Fee Description Fee Page 1	
Account Number	1051	130	2051		Surcharge - late filing fee or oath	
Deposit Account	1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
Name The Director is authorized to: (check all that apply)	1053	130	1053		Non-English specification	
Charge fee(s) indicated below Credit any overpayments	1812	-		-	For filing a request for ex parte reexamination	<b></b>
Charge any additional fee(s) or any underpayment of fee(s)	1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	<b>—</b> Ⅱ
Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.	1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
FEE CALCULATION	1251	110	2251	55	Extension for reply within first month	
1. BASIC FILING FEE	1252	420	2252	210	Extension for reply within second month	
Large Entity Small Entity	1253	950	2253	475	Extension for reply within third month	
Fee Fee Fee Fee Pee Pee Paid Code (\$) Code (\$)	1254	1,480	2254	740	Extension for reply within fourth month	
1001 770 2001 385 Utility filing fee	1255	2,010	2255	1,005	Extension for reply within fifth month	
1002 340 2002 170 Design filing fee	1401	330	2401	165	Notice of Appeal	
1003 530 2003 265 Plant filing fee	1402	330	2402	165	Filing a brief in support of an appeal	<b>—</b>
1004 770 2004 385 Reissue filing fee	1403	290	2403	145	Request for oral hearing	
1005 160 2005 80 Provisional filing fee	1451	1,510	1451	1,510	Petition to institute a public use proceeding	
SUBTOTAL (1) (\$)	1452	110	2452	55	Petition to revive - unavoidable	
2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE	1453	1,330	2453	665	Petition to revive - unintentional	
Fee from	1501		2501		Utility issue fee (or reissue)	
Total Claims	1502	480	2502		Design issue fee	
Independent 2**-	1503	640	2503		Planti ssue fee	
Claims -3 -	1460	130	1460		Petitions to the Commissioner	<b> </b>
	1807	50	1807		Processing fee under 37 CFR 1.17(q)	$\frac{1}{2}$
Large Entity   Small Entity Fee Fee Fee Fee Fee Description	1806	180	1806		Submission of Information Disclosure Stmt 180.	
Code (\$) Code (\$)	8021	40	8021	1 40	Recording each patent assignment per property (times number of properties)	
1202 18 2202 9 Claims in excess of 20 1201 86 2201 43 Independent claims in excess of 3	1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1203 290 2203 145 Multiple dependent claim, if not paid 1204 86 2204 43 ** Reissue independent claims	1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1204 86 2204 43 ** Reissue independent claims over original patent	1801	770	2801	385	Request for Continued Examination (RCE)	
1205 18 2205 9 ** Reissue claims in excess of 20 and over original patent	1802	900	1802	900	Request for expedited examination of a design application	
SUBTOTAL (2) (\$)	Other	fee (sp	ecify) _			
**or number previously paid, if greater; For Reissues, see above	*Redu	iced by	Basic I	Filing F	ee Paid SUBTOTAL (3) (\$) \80 .00	

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Registration No.

(Attorney/Agent)

39.603

SUBMITTED BY

Name (Print/Type)

Signature

NOV 1 0 2003

#### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

Pak Shing Chau, Haw-Jyh Liaw, Jun Kim and Jared L. Zerbe

Assignee:

Rambus, Inc.

Title:

"LOW-LATENCY EQUALIZATION IN MULTI-LEVEL, MULTI-LINE

**COMMUNICATION SYSTEMS**"

Serial No.:

09/654,643

Filed:

09/05/00

Examiner:

Bayard, Emmanuel

Tel:

(703) 308-9573 RECEIVED

Docket No.:

RA-194

Art Unit:

2631

NOV 1 4 2003

**Technology Center 2600** 

Mail Stop Issue Fee Commissioner For Patents P.O. Box 1450 Alexandria, VA 22313-1450

#### SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §1.56, §1.97 and §1.98, Applicants bring the 216 documents listed on the enclosed forms PTO-1449 to the Examiner's attention in the above-captioned application. Citation of the listed documents shall not be construed as:

- 1 an admission that the documents are necessarily prior art with respect to the instant application;
- 2. a representation that a search has been made; or
- 3. an admission that the information cited is, or is considered to be, material to patentability as defined in §1.56(b).

11/13/2003 HVUONG1 00000034 09654643

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Data

Laurie Moreno

Respectfully submitted,

Arthur J. Behiel

Attorney for Applicants

Reg. No. 39,603

		SWENT & T	- SENTE			Sheet 1 of 1	
U.S. Depar	tment of Commerce	Seria	Serial No.: 09/654,643				
				Filir	g Date: 09,	/05/00	
SUPPL	EMENTAL INFORMATI		First Named Inventor: Pak Shing Chau				
				Group	Art Unit:	2631	
"Low-Lat	tency Equalization	on in Multi-Le ation Systems			Examiner Name: Bayard, Emmanuel		
		,			Attorney Docket No.: RA-194		
		3					
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date, If	

			0.5. 1	Patent Documents	5		
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
,	A	4,481,625	11/06/84	Roberts, et al	370	85	
	В	5,534,795	07/09/96	Wert, et al	326	81 REC	EIVED
	С	5,534,798	07/09/96	Phillips, et al	326	108 <b>NOV</b>	1 4 2003
	D	5,663,663	09/02/97	Cao, et al	326	*Technolog	y Center 2600
	E	5,751,168	05/12/98	Speed, III et al	326	83	2000
	F	5,757,712	05/26/98	Nagel, et al	365	226	
	G	5,867,010	02/02/99	Hinedi, et al	323	282	
	Н	5,973,508	10/26/99	Nowak, et al	326	81	
	I	5,986,472	11/16/99	Hinedi, et al	326	68	
	J	6,097,215	08/01/00	Bialas Jr., et al	326	68	
	K	6,140,841	10/31/00	Suh	326	60	
	L	6,160,421	12/12/00	Barna	326	63	
	М	4,748,637	05/31/88	Bishop, et al	375	7	-
	N	5,254,883	10/19/93	Horowitz, et al	307	443	
	0	5,608,755	03/04/97	Rakib	375	219	
	P	5,546,042	08/13/96	Tedrow, et al	327	538	
	Q	5,194,765	03/16/93	Dunlop, et al	307	443	
	R	5,254,883	10/19/93	Horowitz, et al	307	443	

Examiner

Date Considered



Serial No.: 09/654,643
Filing Date: 09/05/00
First Named Inventor: Pak Shing Chau
Group Art Unit: 2631
Examiner Name: Bayard, Emmanuel
Attorney Docket No.: RA-194

#### U.S. Patent Documents

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	S	5,513,327	04/30/96	Farmwald, et al	395	309	
	Т	5,023,488	06/11/91	Gunning	307	475	
	Ŭ	5,483,110	01/09/96	Koide, et al	307	147 RE(	CEIVED
	V	5,287,108	02/15/94	Mayes, et al	341	<sup>156</sup> NO	1 4 2003
	W	5,977,798	11/02/99	Zerbe	329		gy Center 2600
	Х	RE30,182	12/25/79	Howson	325	42	<del>rgy Ochtol 2000 -</del>
	Y	2,912,684	11/10/59	F.G. Steele	340	347	
	Z	3,051,901	08/28/62	R.E. Yaegar	325	38	
	AA	3,078,378	02/19/63	C.H. Burley, et al	307	88.5	,· · · · · · · · · · · · · · · · · · ·
<del></del>	AB	3,267,459	08/16/66	J.S. Chomicki, et al	340	347	
	AC	3,484,559	12/16/69	D.F. Rigby	179	18	
	AD	3,508,076	04/21/70	R.O. Winder	307	235	
	AE	3,510,585	05/05/70	R.B. Stone	325	38	
	AF	3,560,856	02/02/71	Hisashi, Kaneko	375	292	
	AG	3,569,955	03/09/71	Maniere	340	347	
	АН	3,571,725	03/23/71	Kaneko, et al	328	14	
	AI	3,587,088	06/22/71	Franaszek	340	347	
	AJ	3,648,064	03/07/72	Mukai, et al	307	213	

Examiner

Date Considered

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U.S. Depar	tment	of Commerce,	Patent and	Trademark Office	Seri	al No.: 09/	654,643	
					Fili	ng Date: 09,	/05/00	
SUPPL	EMENI		N DISCLOSURI	E STATEMENT BY		t Named Inve Shing Chau	entor:	
				,	Grou	p Art Unit:	2631	
"Low-La	tency		in Multi-Le ion Systems	evel, Multi-Line	Emma	Examiner Name: Bayard, Emmanuel		
						Attorney Docket No.: RA-194		
			U.S. I	Patent Documents	3			
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate	
	AK	3,697,874	10/10/72	Kaneko	325	38 A		
	AL	3,731,199	05/01/73	Tazaki, et al	325	38 A		
	АМ	3,733,550	05/15/73	Tazaki, et al	325	38 A	ECEIVED	

AF	ĸ	3,697,874	10/10/72	Kaneko	325	38 A	
AI	L	3,731,199	05/01/73	Tazaki, et al	325	38 A	
AA A	М	3,733,550	05/15/73	Tazaki, et al	325	38 A	ECEIVED
A	N	3,753,113	08/14/73	Maruta, et al	325	38 A	NOV 1 4 2003
AC	0	3,754,237	08/21/73	de Laage de Meux	340	347 DDTech	nology Center 260
AI	P	3,761,818	09/25/73	Tazaki, et al	325	38 A	
AÇ	Q	3,772,680	11/13/73	Kawai, et al	340	347 DD	
AF	R	3,798,544	03/19/74	Norman	325	38 A	
AS	S	3,832,490	08/27/74	Leonard	178	68	
ΓA	Г	3,860,871	01/14/75	Hinoshita, et al	325	38 B	
AU	U	3,876,944	04/08/75	Mack, et al	325	141	
VA.	V	3,927,401	12/16/75	McIntosh	340	347 DD	
AW	W	3,978,284	08/31/76	Yoshino, et al	178	69.5 R	
AX	Х	3,988,676	10/26/76	Whang	325	38 A	
AY	Y	4,038,564	07/26/77	Hakata	307	205	
AZ	z	4,070,650	01/24/78	Ohashi, et al	340	172	
BA	A.	4,086,587	04/25/78	Lender	340	347 DD	
ВЕ	в	4,097,859	06/27/78	Looschen	340	347 DD	

Examiner

Date Considered

<sup>\*</sup>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

Sheet 4 of 14

U.S. Department of Commerce, Fatent and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194
U.S. Patent Documents	RA-194

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	вс	4,131,761	12/26/78	Giusto	179	15 BY	ECENTED.
	BD	4,181,865	01/01/80	Kohyama	307	361	RECEIVED
	BE	4,373,152	02/08/83	Jacobsthal	340	347	NOV 1 4 2003
	BF	4,382,249	05/03/83	Jacobsthal	340	347 DD <b>Te</b> C	nnology Center 2600
	BG	4,403,330	09/06/83	Meyer	375	4	
	ВН	4,408,135	10/04/83	Yuyama, et al	307	474	
	ВІ	4,408,189	10/04/83	Betts, et al	340	347 DD	
	ВJ	4,528,550	07/09/85	Graves, et al	340	347 DD	
	вк	4,438,491	03/20/84	Constant	364	200	
	BL	4,571,735	02/18/86	Furse	375	20	
	вм	4,602,374	07/22/86	Nakamura, et al	375	17	
	BN	4,628,297	12/09/86	Mita, et al	340	347 DD	
	во	4,779,073	10/18/88	Iketani	341	55	
	ВР	4,805,190	02/14/89	Jaffre, et al	375	17	
	BQ	4,821,286	04/11/89	Graczyk, et al	375	4	
	BR	4,823,028	04/18/89	Lloyd	307	355	
	BS	4,841,301	06/20/89	Ichihara	341	126	
	ВТ	4,860,309	08/22/89	Costelío	375	17	

Examiner

Date Considered

Sheet 5 of 14

U.S. Department of Commerce, and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

#### U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	BU	4,875,049	10/17/89	Yoshida	341	159	
	BV	4,888,764	12/19/89	Haug	370	85.1 <b>R</b>	<b>ECEIVED</b>
	BW	5,003,555	03/26/91	Bergmans	375	12	10V 1 4 2003
	вх	5,045,728	09/03/91	Crafts	307	<sup>475</sup> Tech	nology Center 260
	BY	5,115,450	05/19/92	Arcuri	375	7	
	BZ	5,121,411	06/09/92	Fluharty	375	20	
	CA	5,172,338	12/15/92	Mehrotra, et al	365	185	
	СВ	5,191,330	03/02/93	Fisher, et al	341	56	
	CC	5,230,008	07/20/93	Duch, et al	375	19	
	CD	5,243,625	09/07/93	Verbakel, et al	375	17	
	CE	5,280,500	01/18/94	Mazzola, et al	375	17	
	CF	5,295,155	03/15/94	Gersbach, et al	375	4	
	CG	5,315,175	05/24/94	Langner	307	443	
	СН	5,331,320	07/19/94	Cideciyan, et al	341	56	
	CI	5,408,498	04/18/95	Yoshida	375	286	
	CJ	5,425,056	06/13/95	Maroun, et al	375	316	
	СК	5,426,739	06/20/95	Lin, et al	395	325	
	CL	5,438,593	08/01/95	Karam, et al	375	317	

Examiner

Date Considered

Sheet 6 of 14

U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

#### U.S. Patent Documents

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	СМ	5,459,749	10/17/95	Park	375	286	
	CN	5,471,156	11/28/95	Kim, et al	326	60 <b>K</b>	ECEIVED
	СО	5,473,635	12/05/95	Chevroulet	375	287	NOV 1 4 2003
	CP	5,525,983	06/11/96	Patel, et al	341	57 Tech	nology Center 26
•	CQ	5,663,631	09/02/97	Kajiura, et al	322	29	
	CR	5,640,605	06/17/97	Johnson, et al	395	881	
	CS	5,684,833	11/04/97	Watanabe	375	286	,
	CT	5,740,201	04/14/98	Hui	375	286	
	CU	5,793,815	08/11/98	Goodnow, et al	375	286	
	CV	5,793,816	08/11/98	Hui	375	286	
	CW	5,796,781	08/18/98	DeAndrea, et al	375	288	
	СХ	5,825,825	10/20/98	Altmann, et al	375	293	
	CY	5,872,468	02/16/99	Dyke	327	72	
	CZ	5,892,466	04/06/99	Walker	341	57	
	DA	5,898,734	04/27/99	Nakamura, et al	375	287	
	DB	5,917,340	06/29/99	Manohar, et al	326	82	
	DC	5,933,458	08/03/99	Leurent, et al	375	317	
	DD	5,942,994	08/24/99	Lewiner, et al	341	56	

Examiner

Date Considered

<sup>\*</sup>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

Sheet 7 of 14

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SUPPLI	SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT					First Named Inventor: Pak Shing Chau				
•					Group	Art Unit:	2631			
"Low-Lat	tency		in Multi-Le	evel, Multi-Line	1	Examiner Name: Bayard, Emmanuel				
	•				Attor RA-19	ney Docket	No.:			
			U.S. E	Patent Documents	5					
*Examiner		Document	Date	Name	Class	Subclass	Filing Date,			

#### Date Name Class Subclass Initial Number Ιf Appropriate 5,946,355 08/31/99 Baker 375 286 09/07/99 Sasaki 329 303 DF 5,949,280 DG 5,969,579 10/19/99 Hartke, et al 332 116 NOV 1 4 2003 5,969,648 10/19/99 Garnett 341 56 DH Technology Center 2600 317 DI Emma, et al 6,018,550 01/25/00 375 6,038,260 03/14/00 Emma, et al 375 259 DJ 04/11/00 326 DK 6,049,229 Manohar, et al 83 6,052,390 04/18/00 Deliot, et al 370 258 6,067,326 05/23/00 Jonsson, et al 375 286 DM6,078,627 06/20/00 375 DN Crayford 286 DO 6,048,931 04/11/00 Fujita, et al 525 67 DΡ 6,094,461 07/25/00 Heron 375 317 DO 6,101,561 08/08/00 Beers, et al 710 66 DR 6,114,979 09/05/00 Kim 341 57 DS 6,122,010 09/19/00 Emelko 348 461 DT6,140,841 10/31/00 Suh 326 60 DU 6,195,397 02/27/01 375 Kwon 288 DV5,023,841 06/11/91 Akrout, et al 365 205

Examiner

Date Considered

Sheet 8 of 14

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U.S. Depar	tment	of Commerce	FADEMIN Patent and	Trademark Office	Ser	ial No.: 09/	654,643
					Fil	ing Date: 09,	/05/00
SUPPL	EMENT		ON DISCLOSUR	E STATEMENT BY		st Named Inve Shing Chau	entor:
					Gro	up Art Unit:	2631
"Low-La	tency		n in Multi-Le tion Systems	evel, Multi-Line "		miner Name: I anuel	Bayard,
			Att RA-	orney Docket 194	No.:		
			U.S.	Patent Document	s		
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
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	DX	5,153,459	10/06/92	Park, et al	307	452 R	ECEIVED
	DY	5,373,473	12/13/94	Okumura	365	208	
	DZ	5,508,570	04/16/96	Laber, et al	327	563	NOV 1 4 2003
	EA	5,734,294	03/31/98	Bezzam, et al	327	<sub>552</sub> Tech	hology Center 260
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	EC	4,280,221	07/21/81	Chun, et al	375	17	
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	EG	5,259,002	11/02/93	Carlstedt	375	38	
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U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

#### Foreign Patent Documents

							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
	EP	EP 0 463 316 A1	02.01.92	EP	H04L 12	40	х	
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U.S. Department of Commerce, Patch and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

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						,	<u> </u>
	FF FG FF F	FD A FE JP 08202677 A FF A	FD A 00/11/93 FE JP 08202677 08/09/96 FF A 11/01/96 FF A 07/11/97 FF A 07/30/98 FF A 03/06/87 FF A 04/27/83 FF A 05/16/79 FF A 05/16/79 FM EP 0 352 FM EP 0 352 FM WO 95/31867 11/23/95 FO JP 10200345 A 07/31/98	FD A 00/11/93	FD A 00711/93	FD A 00711/93	FF A

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Technology Center 2600 Sheet 11 of 14 A FRESH M Serial No.: 09/654,643 U.S. Department of Commerce, and Trademark Office Filing Date: 09/05/00 First Named Inventor: SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY Pak Shing Chau APPLICANT Group Art Unit: 2631 "Low-Latency Equalization in Multi-Level, Multi-Line Examiner Name: Bayard, Communication Systems" Emmanuel Attorney Docket No.: RA-194 OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) IBM, Disclosure entitled, "Servo Control of Analog Power Supplies Purpose Interface Card", 4/1/1993, Vol. 36, Issue 4, pages 283-286 Sidiropoulos, Stefanos, et al. "A 700 Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State FS Circuits; Vol. 32, No.5, May 1997; pp. 681-690 Donnelly, Kevin S. et al. "A 660 MB/s Interface Megacell Portable Circuit in 0.3 um-0.7 um CMOS ASIC", IEEE Journal of Solid State Circuits; Vol. 31, No.12; December 1996, pp. 1995-2003 Allen, Arnold O., "Probability, Statistics, and Queueing Theory with FU Computer Science Applications", 2nd Edition, CH 7; pp. 450, 458-459 Chappell, Terry I. et al. "A 2ns Cycle, 4ns Access 512kb CMOS ECL SRAM", FV IEEE International Solid State Circuits Conference 1991; pp. 50-51 Pilo, Harold et al., "A 300 MHz 3.3V 1 Mb SRAM Fabricated in a 0.5 um CMOS Process", IEEE International Solid State Circuits Conference 1996; pp. 148-149 Schumacher, Hans-Jurgen et al., "CMOS Subnanosecond True-ECL Output Buffer", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1; February FX 1990 pp. 150-154. Yang, Tsen-Shau et al., "A 4-ns 4Kx1-bit Two-Port BiCMOS SRAM", IEEE FY Journal of D-State Circuits; Vol. 23, No. 5; October 1988; pp. 1030-1040 Sidiropoulos, Stefanos, et al. "A 700 Mbps/pin CMOS Signalling Interface Using Current Integrating Receivers", IEEE Symposium on VLSI Circuits FZDigest of Technical Papers, 1996; pp 142-143 Bazes, Mel, "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers", IEEE Journal of Solid State Circuits, Vol. 26 No. 2., Februarv 1991 Ishibe, Manabu et al., "High-Speed CMOS I/O Buffer Circuits", IEEE GB Journal of Solid State Circuits, Vol. 27, No. 4, April 1992 Lee, James M. et al., "A 80ns 5V-Only Dynamic RAM", ISSCC Proceedings, GCPaper 12.2 ISSCC 1979.

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Technology Center 2600 Sheet 12 of 14 Serial No.: 09/654,643 ent and Trademark Office U.S. Department of Commerce Filing Date: 09/05/00 First Named Inventor: SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY Pak Shing Chau APPLICANT Group Art Unit: 2631 "Low-Latency Equalization in Multi-Level, Multi-Line Examiner Name: Bayard, Communication Systems" Emmanuel Attorney Docket No.: RA-194 OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Tomasini, Luciano et al. "A Fully Differential CMOS Line Driver for ISDN", IEEE Journal of Solid State Circuits, Vol. 25, No. 2., April 1990. Pages 546-585. Farjad-Rad, Ramin et al., "A 0.4 um CMOS 10-Gb/s 4-PAM Pre-Emphasis Serial Link Transmitter", IEEE Journal of Solid State Circuits, Vol. 34 GG No. 5, pp. 580-585, May 1999. Yeung, Evelina et al., "A 2.4Gbps Per Pin Simultaneous Bidirectional Parallel Link with Per Pin Skew Compensation," ISSCC 2000, in press as of GH 1-9-2000. Portmann C. et al., "A Multiple Vendor 2.5-V DLL for 1.6-GB/s RDRaMs", GI IEEE VLSI Circuits Symposium, June 1999. Moncayo Alfredo, "Bus Design and Analysis at 500 MHz and Beyond", Presented at the High-Performance System Design Conference, 1995. Lau, Benedict et al., " A 2.6-Gbyte/s Multipurpose Chip-to-Chip Interface", IEEE Journal of Solid-State Circuits, Vol. 33, No. 11 pp. 1617-1626, November 1998. Current, Wayne K., "Current-Mode CMOS Multiple-Valued Logic Circuits", GT. IEEE Journal of Solid-State Circuits, Vol. 29, No. 2, pp. 95-107, February 1994. Dally, William J. et al., "Digital Systems Engineering", Cambridge GM University Press, New York, NY, 1998, Index, pp. 344-347 and pg. 352. Farjad-Rad, Ramin et al., "An Equalization Scheme for 10Gb/s 4-PAM Signaling Over Long Cables," Presentation Center for Integrated Systems, Department of Electrical Engineering, Stanford University, July 28, 1997 Vranesic, Z.G. "Multivalued Signalling in Daisy Chain Bus Control", Proceedings of the Ninth International Symposium on Multiple-Valued Logic, Bath, England, pp. 14-18 IBM Technical Disclosure Bulletin, "Use of Multibit Encoding to Increase GP Linear Recording Densities in Serially Recorded Records," June 1967. pp. IBM Technical Disclosure Bulletin, "Coding for Data Transmission", GO January 1968, pp. 1295-1296 IBM Technical Disclosure Bulletin, "Clock Recovery Circuit," July 1969, GR pp. 219-220 IBM Technical Disclosure Bulletin, "Transmission by Data Encoding," GS November 1970, pg. 1519 Date Considered Examiner \*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered.

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Sheet 13 of 14 Technology Center 2600 Serial No.: 09/654,643 U.S. Department of Commerce, Patent and Trademark Office Filing Date: 09/05/00 First Named Inventor: SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY Pak Shing Chau APPLICANT Group Art Unit: 2631 Examiner Name: Bayard, "Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems" Emmanuel Attorney Docket No.: RA-194 OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) IBM Technical Disclosure Bulletin, "Bidirectional Communications within a Binary Switching System", February 1976, pp. 2865-2866 IBM Technical Disclosure Bulletin, "Multilevel Bidirectional Signal GU Transmission", February 1976, pp. 2867-2868. IBM Technical Disclosure Bulletin, "Multilevel Signal Transfers," October GV 1978, pp. 1798-1800 IBM Technical Disclosure Bulletin, "Circuit for Multilevel Logic GW Implementation", February 1981, pp 4206-4207 IBM Technical Disclosure Bulletin, "Multi Level Logic Testing", April 1983, pp. 5903-5904 IBM Technical Disclosure Bulletin, "Push-Pull Multi-Level Driver Circuit GY for Input-Output Bus", September 1985, pp. 1649-1650 IBM Technical Disclosure Bulletin, "Multilevel CMOS Sense Amplifier", GΖ August 1986, pp. 1280-1281 IBM Technical Disclosure Bulletin, "Multi-Level Encoded High Bandwidth HA Bus", November 1992, pp. 444-446 IBM Technical Disclosure Bulletin, "High Speed Complimentary Metal Oxide HB Semiconductor Input/Output Circuits", February 1995, pp. 111 of 111- 114. IBM Technical Disclosure Bulletin, "Common Front End Bus for High-HC Performance Chip-to-Chip Communication", April 1995, pp. 443-444 IBM Technical Disclosure Bulletin, "High Performance Impedance Controlled HD CMOS Drive", April 1995, pp. 445-446 IBM Technical Disclosure Bulletin, "3-State Decoder for External 3-State HE Buffer", April 1995, pg. 477 Matick, Richard E., "Transmission Lines for Digital and Communication Networks: An Introduction to Transmission Lines, High-Frequency and High-Speed Pulse Characteristics and Applications," IEEE Press, New York, 1995, pp. 268-269 Date Considered Examiner \*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered.

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